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(54) **PIXEL CIRCUIT AND LIGHT EMITTING DISPLAY**

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(57) **ABSTRACT**

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A pixel circuit for a light emitting display. Adjacent pixels of the light emitting display coupled to one scan line share one first power supply line. A driving circuit in each pixel circuit drives first and second organic light emitting diodes (OLEDs). A switching circuit is coupled between the first and second OLEDs and the driving circuit to sequentially control the driving of the first and second OLEDs. Because two adjacent pixel circuits share one pixel power supply line and a plurality of OLEDs are coupled to one pixel circuit, it is possible to reduce the number of pixel circuits and the number of wiring lines of the light emitting display. Other circuit elements may also be shared between adjacent pixel circuits. Reducing the wiring and other elements of the pixel circuits makes it possible to increase the aperture ratio of the light emitting display.

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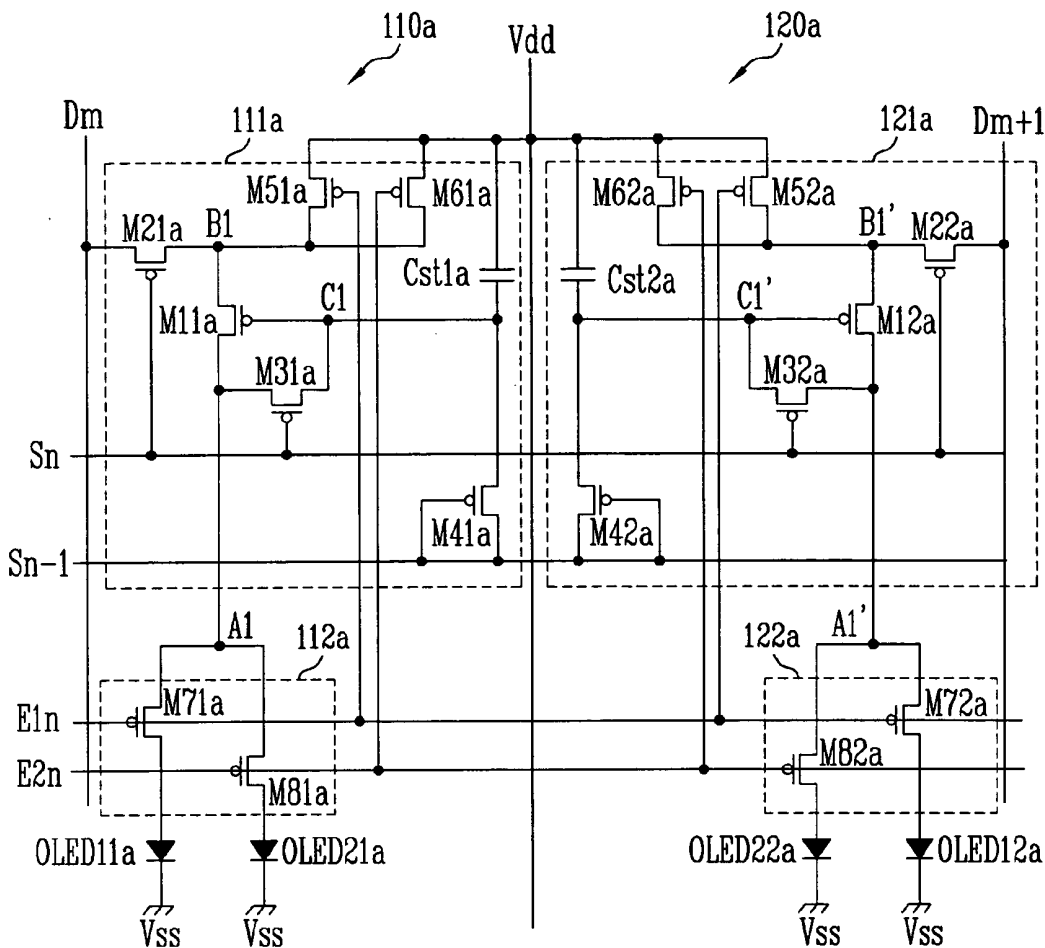


FIG. 1
(PRIOR ART)

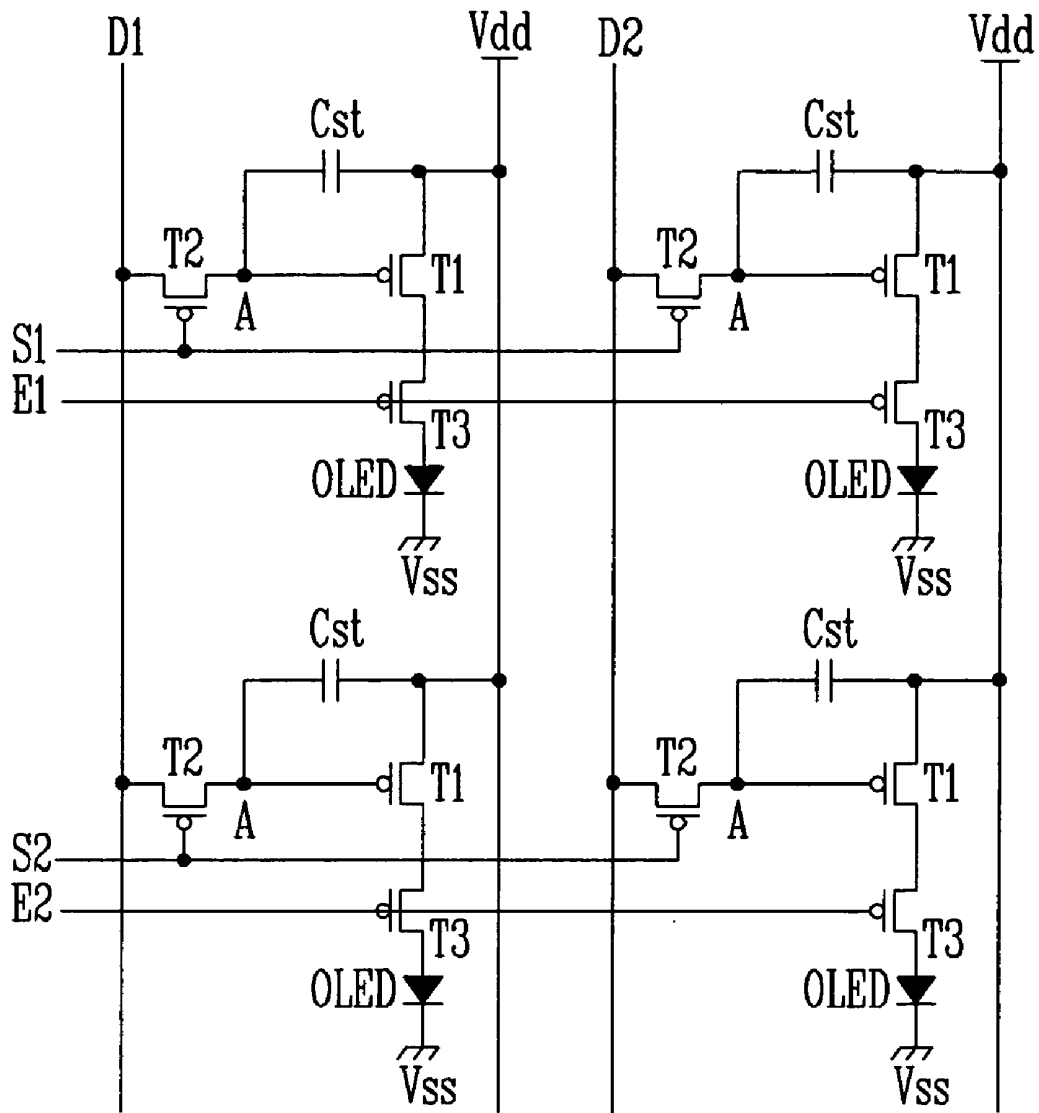


FIG. 2

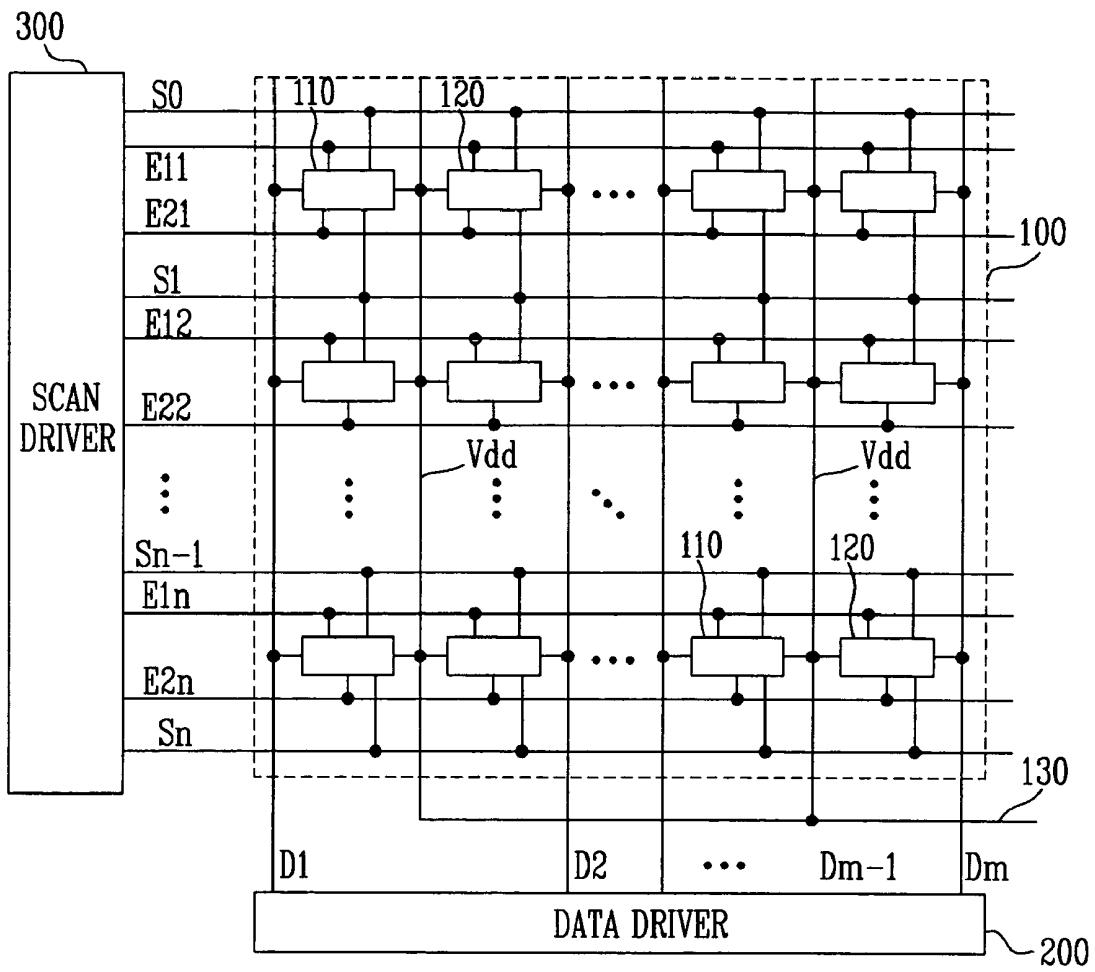


FIG. 3

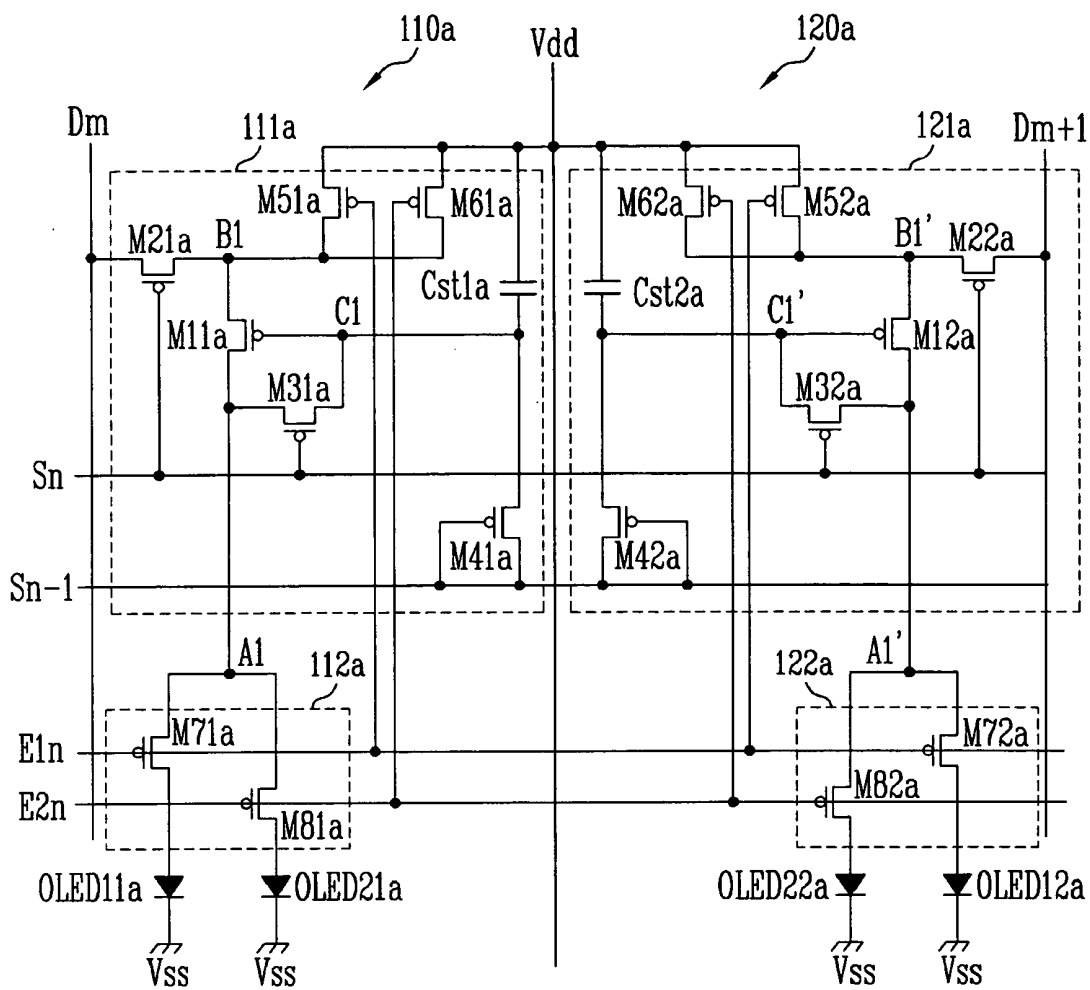


FIG. 4

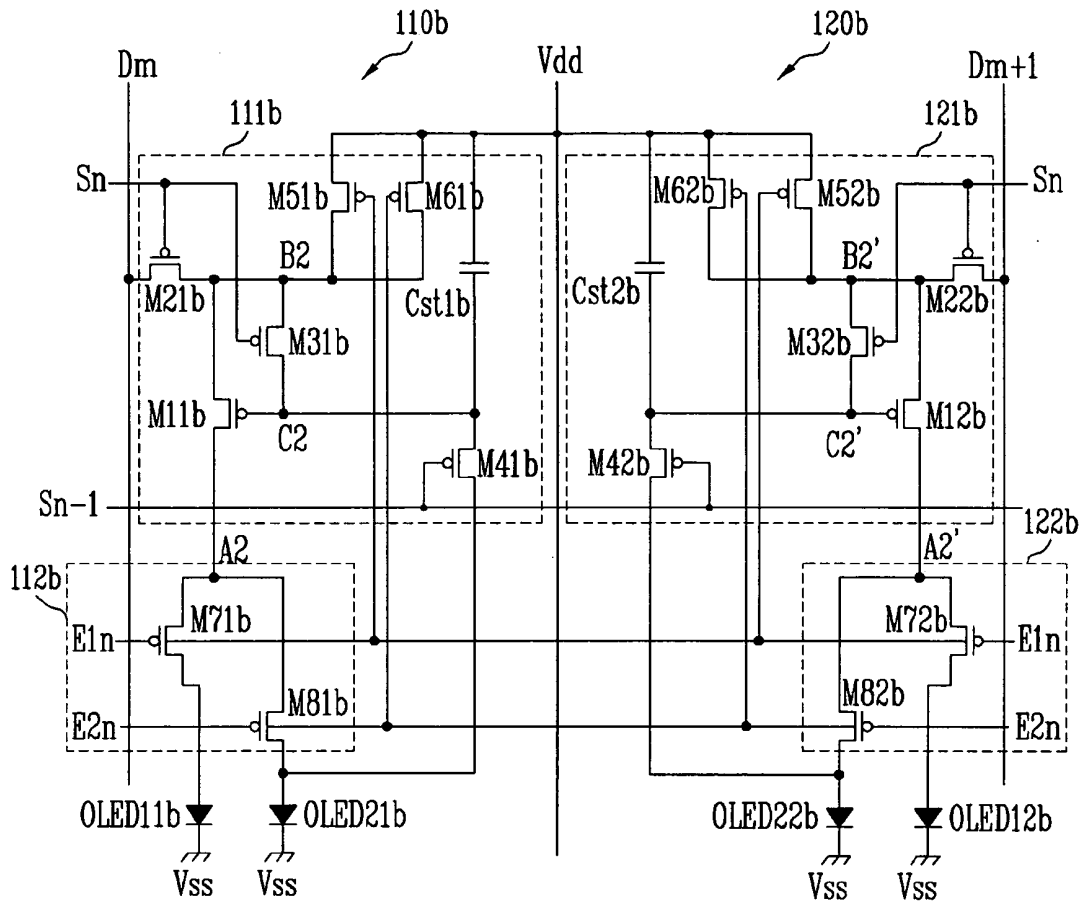


FIG. 5

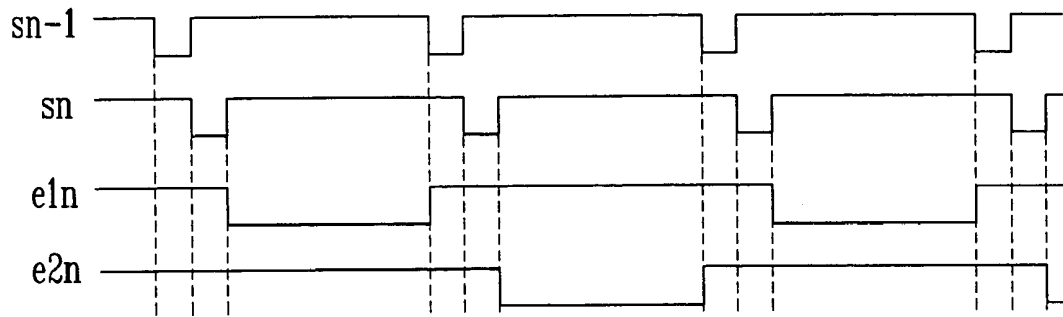


FIG. 6

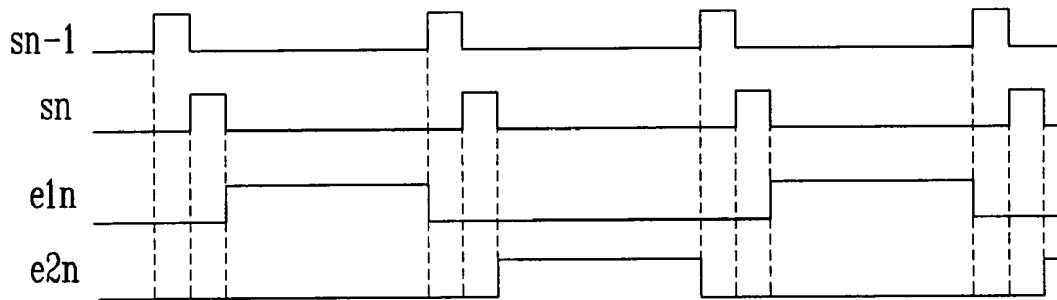
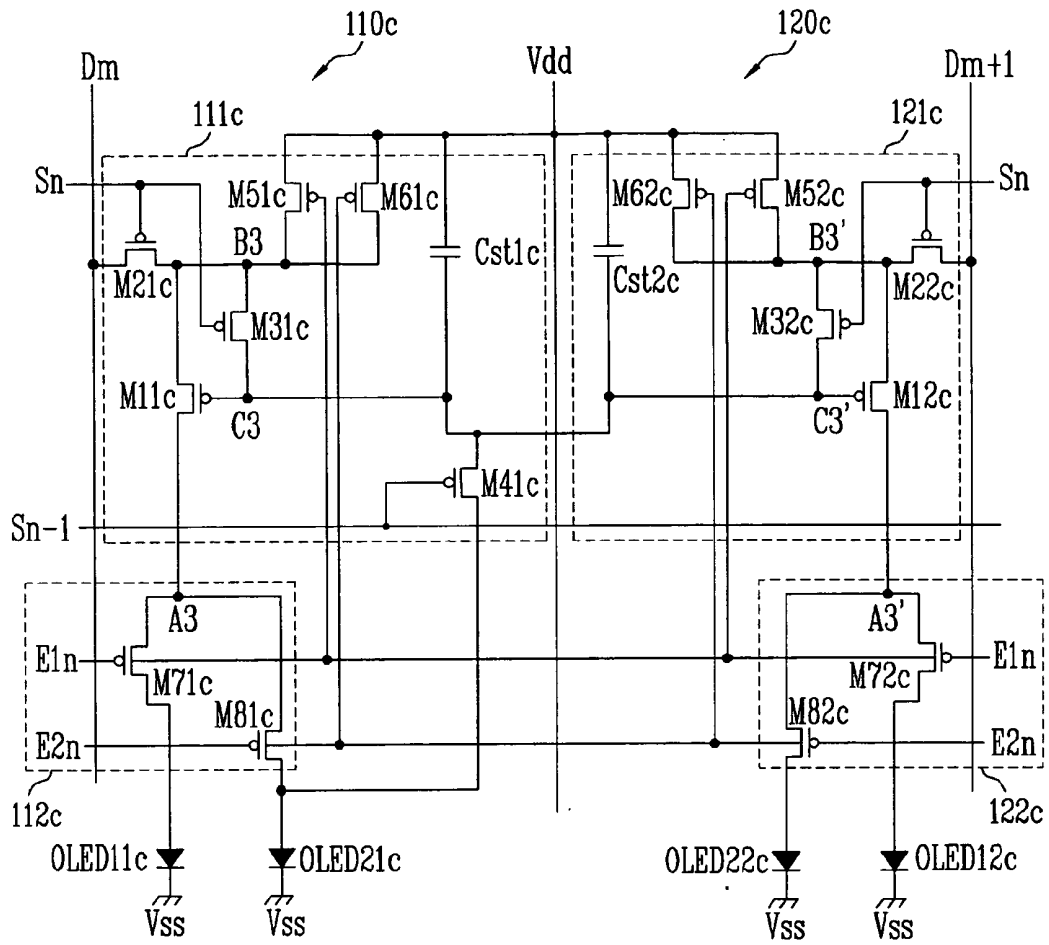


FIG. 7



PIXEL CIRCUIT AND LIGHT EMITTING DISPLAY**CROSS-REFERENCE TO RELATED APPLICATION**

[0001] This application claims priority to and the benefit of Korean Patent Application No. 10-2004-95984, filed on Nov. 22, 2004, in the Korean Intellectual Property Office, the entire content of which is incorporated herein by reference.

BACKGROUND

[0002] 1. Field of the Invention

[0003] The present invention relates to a light emitting display, and more particularly to a pixel circuit coupled to a plurality of organic light emitting diodes (OLED) that emit light so that it is possible to improve the aperture ratio of the light emitting display, to compensate for the threshold voltage, and to thus make brightness uniform and a light emitting display using the same.

[0004] 2. Discussion of Related Art

[0005] Recently, various flat panel displays of lower weight and volume compared with cathode ray tubes (CRT) have been developed. In particular, light emitting displays having improved luminous efficiency, brightness, view angle, and high response speed are spotlighted.

[0006] In an OLED, an emission layer made of a thin film that emits light is positioned between a cathode electrode and an anode electrode. Electrons and holes are injected into the emission layer and are recombined to generate exciters at a reduced overall energy. Light is emitted as a result of this recombination.

[0007] The emission layer of the OLED may be formed from organic or inorganic material. The OLED is divided into organic and inorganic OLEDs according to the type of the emission layer.

[0008] **FIG. 1** is a circuit diagram illustrating a part of a conventional light emitting display. Four adjacent pixels are shown that each include an OLED and a pixel circuit. The pixel circuit includes a first transistor T1, a second transistor T2, a third transistor T3, and a capacitor Cst. Each of the first, second, and third transistors T1, T2, T3 includes a gate, a source, and a drain and the capacitor Cst includes a first electrode and a second electrode.

[0009] Because the pixels all have the same circuit, only the left top pixel will be described. The source of the first transistor T1 is coupled to a power supply line Vdd, the drain of the first transistor T1 is coupled to the source of the third transistor T3, and the gate of the first transistor T1 is coupled to a first node A. The first node A is coupled to the drain of the second transistor T2. The source of the second transistor T2 is coupled to a data line D1, the drain of the second transistor T2 is coupled to the first node A, and the gate of the second transistor T2 is coupled to a first scan line S1. The second transistor T2 transmits a data signal to the first node A in response to the scan signal applied to its gate. The first transistor T1 supplies current corresponding to the data signal to the OLED.

[0010] The source of the third transistor T3 is coupled to the drain of the first transistor T1, the drain of the third transistor T3 is coupled to the anode electrode of the OLED,

and the gate of the third transistor T3 is coupled to an emission control line E1 to respond to an emission control signal. Therefore, the third transistor T3 controls the flow of current that flows from the first transistor T1 to the OLED in response to the emission control signal to control emission of the OLED.

[0011] The first electrode of the capacitor Cst is coupled to the power supply line Vdd and the second electrode of the capacitor Cst is coupled to the first node A. The capacitor Cst is charged according to the data signal and applies a signal to the gate of the first transistor T1 during one frame and therefore maintains the first transistor T1 operating during the one frame.

[0012] However, in the conventional pixel circuit for the light emitting display, because each OLED is driven by a pixel circuit of its own, a plurality of pixel circuits are necessary to drive a plurality of OLEDs. This design feature increases the number of pixel circuits that form the display.

[0013] Also, because one emission control line and a pixel power supply line are coupled to each pixel row, wiring lines become complicated and the aperture ratio of the light emitting display deteriorates.

[0014] Therefore, there is a need for an alternative design that reduces the number of the pixel circuits and simplifies the arrangement of the wiring lines.

SUMMARY OF THE INVENTION

[0015] Accordingly, one aspect of the present invention provides light emitting displays, in which two adjacent pixel circuits coupled to one scan line share one pixel power supply line and a plurality of OLEDs are coupled to one pixel circuit so that it is possible to reduce the number of pixel circuits and the number of wiring lines of the light emitting display and thus improve the aperture ratio of the light emitting display.

[0016] The foregoing and/or other aspects of the present invention are achieved by providing a light emitting display including an image display unit coupled to a plurality of scan lines, a plurality of data lines, a plurality of emission control lines, and a plurality of first power supply lines and including a plurality of pixels formed in the regions defined by the scan lines and the data lines. Each of first and second adjacent pixels coupled to one scan line and one first power supply line among the plurality of pixels includes first and second OLEDs, a driving circuit commonly coupled to the first and second OLEDs to drive the first and second OLEDs, and a switching circuit coupled between the first and second OLEDs and the driving circuit to sequentially control the driving of the first and second OLEDs. The driving circuit includes a first transistor for receiving the first power source corresponding to a first voltage applied to the gate to selectively supply current to the first and second OLEDs, a second transistor for selectively transmitting a data signal to the first electrode of the first transistor by a first scan signal, a third transistor for selectively flowing electric current to the first transistor so that the first transistor serves as a diode by the first scan signal, a capacitor for storing the voltage applied to the gate of the first transistor while a data voltage is applied to the first electrode of the first transistor and for maintaining the stored voltage in the gate of the first transistor in the period where the OLEDs emit light, a fourth

transistor for selectively transmitting an initializing signal to the capacitor by a second scan signal, a fifth transistor for selectively transmitting the first power source to the first transistor by the first emission control signal, and a sixth transistor for selectively transmitting the first power source to the first transistor by the second emission control signal.

[0017] According to another aspect of the present invention, there is provided a light emitting display including first and second adjacent pixels coupled to one scan line. Each of the first and second pixels includes first and second OLEDs for receiving a current to emit light, a first transistor whose drain is coupled to a first node, whose source is coupled to a second node, and whose gate is coupled to a third node, a second transistor whose source is coupled to a data line, whose drain is coupled to the second node, and whose gate is coupled to a first scan line, a third transistor whose source is coupled to the first node, whose drain is coupled to the third node, and whose gate is coupled to the first scan line, a fourth transistor whose source is coupled to an initializing line, whose drain is coupled to the third node, and whose gate is coupled to a second scan line, a capacitor whose first electrode is coupled to a first power source and whose second electrode is coupled to the third node, a fifth transistor whose source is coupled to the first power supply line, whose drain is coupled to the second node, and whose gate is coupled to a first emission control line, a sixth transistor whose source is coupled to the first power supply line, whose drain is coupled to the second node, and whose gate is coupled to a second emission control line, a seventh transistor whose source is coupled to the first node, whose drain is coupled to the first OLED, and whose gate is coupled to the first emission control line, and an eighth transistor whose source is coupled to the first node, whose drain is coupled to the second OLED, and whose gate is coupled to the second emission control line.

[0018] According to another aspect of the present invention, there is provided a light emitting display including first and second adjacent pixels coupled to one scan line. Each of the first and second pixels includes first and second OLEDs for receiving current to emit light, a first transistor whose drain is coupled to a first node, whose source is coupled to a second node, and whose gate is coupled to a third node, a second transistor whose source is coupled to a data line, whose drain is coupled to the second node, and whose gate is coupled to a first scan line, a third transistor whose source is coupled to the second node, whose drain is coupled to the third node, and whose gate is coupled to the first scan line, a fourth transistor whose source is coupled to an initializing line, whose drain is coupled to the third node, and whose gate is coupled to a second scan line, a capacitor whose first electrode is coupled to a first power source and whose second electrode is coupled to the third node, a fifth transistor whose source is coupled to the first power supply line, whose drain is coupled to the second node, and whose gate is coupled to a first emission control line, a sixth transistor whose source is coupled to the first power supply line, whose drain is coupled to the second node, and whose gate is coupled to a second emission control line, a seventh transistor whose source is coupled to the first node, whose drain is coupled to the first OLED, and whose gate is coupled to the first emission control line, and an eighth transistor whose source is coupled to the first node, whose drain is coupled to the second OLED, and whose gate is coupled to the second emission control line.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] FIG. 1 is a circuit diagram illustrating a part of a conventional light emitting display.

[0020] FIG. 2 illustrates the structure of a light emitting display according to a first embodiment of the present invention.

[0021] FIG. 3 is a circuit diagram illustrating a first embodiment of the pixel used for the light emitting display of the present invention.

[0022] FIG. 4 is a circuit diagram illustrating a second embodiment of the pixel used for the light emitting display of the present invention.

[0023] FIG. 5 illustrates waveforms that describe the operation of the pixel of FIGS. 3 and 4.

[0024] FIG. 6 illustrates waveforms that describe the operation of the pixel of FIGS. 3 and 4 using NMOS transistors.

[0025] FIG. 7 is a circuit diagram illustrating a third embodiment of the pixel used for the light emitting display of the present invention.

DETAILED DESCRIPTION

[0026] FIG. 2 illustrates a light emitting display according to a first embodiment of the present invention. The light emitting display includes an image display unit 100, a data driver 200, and a scan driver 300.

[0027] The image display unit 100 includes a plurality of pixels 110, 120 including a plurality of OLEDs, a plurality of scan lines $S_0, S_1, S_2, \dots, S_{n-1}, S_n$ arranged in a row direction, a plurality of first emission control lines $E_{11}, E_{12}, \dots, E_{1n-1}, E_{1n}$ and second emission control lines $E_{21}, E_{22}, \dots, E_{2n-1}, E_{2n}$ arranged in the row direction, a plurality of data lines $D_1, D_2, \dots, D_{m-1}, D_m$ arranged in a column direction, and a plurality of pixel power supply lines V_{dd} for supplying pixel power.

[0028] Each one pixel power supply line V_{dd} is simultaneously coupled to two adjacent pixels 110 (or to two adjacent pixels 120) in the row direction so that the number of required pixel power supply lines V_{dd} is reduced to half of the number of pixels. Therefore, it is possible to reduce the number of wiring lines required for the image display unit 100. The pixel power supply lines V_{dd} receive pixel power source from an external power source 130.

[0029] The pixels 110, 120 receive a scan signal of a present or first scan line S_n and a scan signal of a previous or second scan line S_{n-1} through the scan lines $S_0, S_1, S_2, \dots, S_{n-1}, S_n$ and generate driving currents corresponding to data signals by the data signals transmitted from data lines $D_1, D_2, \dots, D_{m-1}, D_m$. The driving currents are transmitted to the OLEDs by first and second emission control signals transmitted through the first emission control lines $E_{11}, E_{12}, \dots, E_{1n-1}, E_{1n}$ and the second emission control lines $E_{21}, E_{22}, \dots, E_{2n-1}, E_{2n}$. Note that the number of scan lines $S_0 \dots S_n$ is one more than the number of first or second emission control lines $E_{11} \dots E_{1n}$ or $E_{21} \dots E_{2n}$.

[0030] The data driver 200 is coupled to the data lines $D_1, D_2, \dots, D_{m-1}, D_m$ to transmit the data signals to the image display unit 100. Each one data line sequentially transmits red, green, and blue data.

[0031] The scan driver 300, shown in the embodiment of FIG. 2 to be located on the side of the image display unit 100, is coupled to the scan lines $S_0, S_1, S_2, \dots, S_{n-1}, S_n$, the first emission control lines $E_{11}, E_{12}, \dots, E_{1n-1}, E_{1n}$, and the second emission control lines $E_{21}, E_{22}, \dots, E_{2n-1}, E_{2n}$ to sequentially transmit the scan signals and the emission control signals to the image display unit 100.

[0032] FIG. 3 is a circuit diagram illustrating a first embodiment of the pixel used for the light emitting display of the present invention. The pixels of the first embodiment include two adjacent pixel circuits 110a, 120a coupled to the same two scan lines S_n, S_{n-1} . The left pixel is referred to as a first pixel 110a and the right pixel is referred to as a second pixel 120a.

[0033] Each of the first and second pixels 110a, 120a include a driving circuit and a switching circuit. The driving circuit 111a, 121a includes elements that are coupled to the scan lines S_n, S_{n-1} and are driven by the scan signals s_n, s_{n-1} . The switching circuit 112a, 122a includes switching elements that are coupled to the emission control lines E_{1n}, E_{2n} and are driven by the emission control signals e_{1n}, e_{2n} . The switching circuit 112a, 122a couples the driving circuit 111a, 121a to the OLEDs and controls the flow of current to these OLEDs.

[0034] In the first pixel 110a, the drain of the first transistor M11a is coupled to a first node A1, the source of the first transistor M11a is coupled to a second node B1, and the gate of the first transistor M11a is coupled to a third node C1 so that current flows from the second node B1 to the first node A1 in response to the voltage of the third node C1.

[0035] The source of the second transistor M21a is coupled to the data line D_m , the drain of the second transistor M21a is coupled to the second node B1, and the gate of the second transistor M21a is coupled to the first scan line S_n . The second transistor M21a performs a switching operation by a first scan signal s_n transmitted through the first scan line S_n and selectively transmits the data signal transmitted through the data line D_m to the second node B1.

[0036] The source of the third transistor M31a is coupled to the first node A1, the drain of the third transistor M31a is coupled to the third node C1, and the gate of the third transistor M31a is coupled to the first scan line S_n . Once the first scan signal s_n is transmitted through the first scan line S_n , the potential of the first node A1 is made equal to the potential of the third node C1 and the first transistor M11 becomes coupled like a diode. As a result, electric current flows through the first transistor M11a.

[0037] The source and gate of the fourth transistor M41a are coupled to the second scan line S_{n-1} and the drain of the fourth transistor M41a is coupled to the third node C1 so that the fourth transistor M41a transmits an initializing signal to the third node C1. The initializing signal is the second scan signal s_{n-1} input to the row that, by one row, precedes the row to which the first scan signal s_n is input. The initializing second scan signal s_{n-1} is transmitted through the second scan line S_{n-1} . The second scan line S_{n-1} is the scan line coupled to the row that, by one row, precedes the row to which the first scan line S_n is coupled.

[0038] The source of the fifth transistor M51a is coupled to the pixel power supply line Vdd, the drain of the fifth transistor M51a is coupled to the second node B1, and the

gate of the fifth transistor M51a is coupled to the first emission control line E_{1n} . The fifth transistor M51a selectively transmits the power from the pixel power supply line Vdd to the second node B1 in response to a first emission control signal e_{1n} transmitted through the first emission control line E_{1n} .

[0039] The source of the sixth transistor M61a is coupled to the pixel power supply line Vdd, the drain of the sixth transistor M61a is coupled to the second node B1, and the gate of the sixth transistor M61a is coupled to the second emission control line E_{2n} so that the sixth transistor M61a selectively transmits the pixel power source to the second node B1 by the second emission control signal e_{2n} transmitted through the second emission control line E_{2n} .

[0040] The source of the seventh transistor M71a is coupled to the first node A1, the drain of the seventh transistor M71a is coupled to the first OLED OLED11a, and the gate of the seventh transistor M71a is coupled to the first emission control line E_{1n} . In response to the first emission control signal e_{1n} transmitted through the first emission control line E_{1n} , the seventh transistor M71a selectively transmits the current that flows through the first node A1 to the first OLED OLED11a, to cause the first OLED OLED11a to emit light.

[0041] The source of the eighth transistor M81a is coupled to the first node A1, the drain of the eighth transistor M81a is coupled to the second OLED OLED21a, and the gate of the eighth transistor M81a is coupled to the second emission control line E_{2n} .

[0042] In response to the second emission control signal e_{2n} transmitted through the second emission control line E_{2n} , the eighth transistor M81a transmits current that flows through the first node A1 to the second OLED OLED21a to emit light from the second OLED OLED21a.

[0043] The first electrode of the capacitor Cst1a is coupled to the pixel power supply line Vdd and the second electrode of the capacitor Cst1a is coupled to the third node C1. As a result, the capacitor Cst1a is initialized by the initializing signal transmitted to the third node C1 through the fourth transistor M41a. Also, the voltage corresponding to the data signal is stored and is transmitted to the third node C1. Therefore, the gate voltage of the first transistor M1a is maintained for a predetermined time.

[0044] The second pixel 120a has the same structure as the first pixel 110a. The second pixel 120a receives power through the pixel power supply line Vdd to which the first pixel 110a is also coupled. The second pixel 120a receives a data signal through the second data line D_{m+1} . The two adjacent pixels 110a, 120a coupled to one scan line share one pixel power source. So, it is possible to reduce the number of pixel power supply lines Vdd.

[0045] FIG. 4 is a circuit diagram illustrating a second embodiment of the pixel circuit used for the light emitting display of the present invention. The pixels including two adjacent pixel circuits coupled to one scan line are illustrated. In the second pixel circuit, the left pixel is referred to as the first pixel 110b and the right pixel is referred to as the second pixel 120b.

[0046] Each of the first and second pixels 110b, 120b include a driving circuit and a switching circuit. The driving

circuit **111b**, **121b** includes elements that are coupled to the scan lines S_n , S_{n-1} and are driven by the scan signals s_n , s_{n-1} . The switching circuit **112b**, **122b** includes switching elements that are coupled to the emission control lines E_{1n} , E_{2n} and are driven by the emission control signals e_{1n} , e_{2n} . The switching circuit **112b**, **122b** couples the driving circuit **111b**, **121b** to the OLEDs and controls the flow of current to these OLEDs.

[0047] In the first pixel **110b**, the drain of the first transistor **M1b** is coupled to a first node **A2**, the source of the first transistor **M1b** is coupled to a second node **B2**, and the gate of the first transistor **M11b** is coupled to a third node **C2**. Current flows from the second node **B2** to the first node **A2** in response to the voltage of the third node **C2**.

[0048] The source of the second transistor **M21b** is coupled to the data line D_m , the drain of the second transistor **M21b** is coupled to the second node **B2**, and the gate of the second transistor **M21b** is coupled to the first scan line S_n . The second transistor **M21b** performs a switching operation in response to the first scan signal s_n transmitted through the first scan line S_n to selectively transmit the data signal transmitted through the data line D_m to the second node **B2**.

[0049] The source of the third transistor **M31b** is coupled to the second node **B2**, the drain of the third transistor **M31b** is coupled to the third node **C2**, and the gate of the third transistor **M31b** is coupled to the first scan line S_n so that the potential of the second node **B2** is made equal to the potential of the third node **C2** by the first scan signal s_n transmitted through the first scan line S_n . Therefore, electric current flows through the first transistor **M11b** diode connecting the first transistor **M11b**.

[0050] The source of the fourth transistor **M41b** is coupled to the anode electrode of the OLED**21b**, the gate of the fourth transistor **M41b** is coupled to the second scan line S_{n-1} , and the drain of the fourth transistor **M41b** is coupled to the third node **C2**. As a result, the fourth transistor **M41b** transmits an initializing signal to the third node **C2**. The initializing signal is the voltage applied to the OLED**21b** when no current flows to the OLED**21b**. The voltage applied to the OLED**21b** is transmitted to the third node **C2** in response to the second scan signal s_{n-1} transmitted through the second scan line S_{n-1} .

[0051] The source of the fifth transistor **M51b** is coupled to the pixel power supply line V_{dd} , the drain of the fifth transistor **M51b** is coupled to the second node **B2**, and the gate of the fifth transistor **M51b** is coupled to the first emission control line E_{1n} . The fifth transistor **M51b** selectively transmits the pixel power source to the second node **B2** by the first emission control signal e_{1n} transmitted through the first emission control line E_{1n} .

[0052] The source of the sixth transistor **M61b** is coupled to the pixel power supply line V_{dd} , the drain of the sixth transistor **M61b** is coupled to the second node **B2**, and the gate of the sixth transistor **M61b** is coupled to the second emission control line E_{2n} . The sixth transistor **M61b** selectively transmits the pixel power source to the second node **B2** in response to the second emission control signal e_{2n} transmitted through the second emission control line E_{2n} .

[0053] The source of the seventh transistor **M71b** is coupled to the first node **A2**, the drain of the seventh

transistor **M71** is coupled to the first OLED **OLED11b**, and the gate of the seventh transistor **M71b** is coupled to the first emission control line E_{1n} . The seventh transistor **M71b** selectively transmits the current that flows through the first node **A2** to the first OLED **OLED11b** in response to the first emission control signal e_{1n} transmitted through the first emission control signal E_{1n} to emit light from the first OLED **OLED11b**.

[0054] The source of the eighth transistor **M81b** is coupled to the first node **A2**, the drain of the eighth transistor **M81b** is coupled to the second OLED **OLED21b**, and the gate of the eighth transistor **M81b** is coupled to the second emission control line E_{2n} . The eighth transistor **M81b** transmits current that flows through the first node **A** to the second OLED **OLED21b** in response to the second emission control signal e_{2n} transmitted through the second emission control line E_{2n} to emit light from the second OLED **OLED21b**.

[0055] The first electrode of the capacitor **Cst1b** is coupled to the pixel power supply line V_{dd} and the second electrode of the capacitor **Cst1b** is coupled to the third node **C2**. As a result, the capacitor **Cst1b** is initialized by the initializing signal transmitted to the third node **C2** through the fourth transistor **M41b** and the voltage corresponding to the data signal is stored and is transmitted to the third node **C2**. Therefore, the gate voltage of the first transistor **M11b** is maintained for a predetermined time.

[0056] The second pixel **120b** has the same structure as the first pixel **110b** and receives power source through the same pixel power supply line to which the first pixel **110b** is coupled. The second pixel **120b**, however, receives its data signal through the second data line D_{m+1} . The two adjacent pixels coupled to one scan line share one pixel power source so that it is possible to reduce the number of pixel power supply lines.

[0057] FIG. 5 illustrates waveforms that describe the operation of the pixel of FIGS. 3 and 4. The first pixel of the first and second embodiments of the pixel circuit **110a**, **110b**, **110c** is operated by the first and second scan signals s_n and s_{n-1} and the first and second emission control signals e_{1n} and e_{2n} .

[0058] First, the fourth transistor **M41a**, **M41b** is turned on by the second scan signal s_{n-1} allowing the initializing signal to be transmitted to the capacitor **Cst1a**, **Cst1b** and to initialize the capacitor.

[0059] The second and third transistors **M21a**, **M21b** and **M31a**, **M31b** are turned on by the first scan signal s_n so that the potential of the second node **B1**, **B2** is made equal to the potential of the third node **C1**, **C2**. Therefore, electric current flows through the first transistor **M11a**, **M11b** so that the first transistor **M11a**, **M11b** serves as a diode and the data signal is transmitted to the second node **B1**, **B2** through the second transistor **M21a**, **M21b**. The data signal is also transmitted to the second electrode of the capacitor **Cst1a**, **Cst1b** through the second transistor **M21a**, **M21b**, the first transistor **M11a**, **M11b**, and the third transistor **M31a**, **M31b** so that the voltage corresponding to difference between the data signal and the threshold voltage is applied to the second electrode of the capacitor **Cst1a**, **Cst1b**.

[0060] After the first scan signal s_n transits to the high level, when the first emission control signal e_{1n} transits to the low level and is maintained in the low level for a period

of time, the fifth and seventh transistors **M51a**, **M51b** and **M71a**, **M71b** are turned on by the first emission control signal **e1n** so that a voltage corresponding to EQUATION 1 is applied between the gate and source of the first transistor **M11a**, **M11b**.

$$V_{gs}=(V_{data}-V_{th})-V_{dd} \quad [\text{EQUATION 1}]$$

[0061] where, V_{gs} , V_{dd} , V_{data} , and V_{th} represent the voltage between the gate electrode and the source electrode of the first transistor **M11a**, **M11b**, a pixel power source voltage, the voltage of the data signal, and the threshold voltage of the first transistor **M11a**, **M11b**, respectively.

[0062] Therefore, the current obtained by EQUATION 2 flows to the first node **A1**, **A2**.

[0063] [EQUATION 2]

$$\begin{aligned} I &= \frac{\beta}{2}(V_{gs} - V_{th})^2 \\ &= \frac{\beta}{2}(V_{data} - V_{dd} + V_{th} - V_{th})^2 \\ &= \frac{\beta}{2}(V_{data} - V_{dd})^2 \end{aligned}$$

[0064] where, I , V_{gs} , V_{dd} , V_{th} , and V_{data} represent the current that flows through the first and second OLEDs, the voltage applied to the gate of the first transistor **M11a**, **M11b**, the voltage of the pixel power source through the power source line, the threshold voltage of the first transistor **M11a**, **M11b**, and the voltage of the data signal, respectively.

[0065] EQUATION 2 is independent of V_{th} . Therefore, the current I flows to the first node **A1**, **A2** regardless of the threshold voltage of the first transistor **M11a**, **M11b**.

[0066] Then, the voltage value corresponding to difference between the voltage of the pixel power source through the power source line V_{dd} and the data signal V_{data} is stored in the capacitor **Cst1a**, **Cst1b** by the first and second scan signals s_n and s_{n-1} ; the voltage V_{sg} corresponding to EQUATION 1 is transmitted between the source and gate of the first transistor **M11a**, **M11b**, the sixth and eighth transistors **M61a**, **M61b** and **M81a**, **M81b** are turned on by the second emission control signal e_{2n} , and the current I corresponding to the EQUATION 2 flows to the second OLED **OLED21a**, **OLED21b**.

[0067] Next, the first emission signal e_{1n} goes high and the second emission signal e_{2n} goes low. Because the first emission control signal e_{1n} is in the high level and the second emission control signal e_{2n} is in the low level, the seventh transistor **M71a**, **M71b** is turned off and the eighth transistor **M81a**, **M81b** is turned on so that the current flows to the second OLED **OLED21a**, **OLED21b** through the eighth transistor **M81a**, **M81b**.

[0068] Therefore, one pixel circuit controls the two OLEDs and the two adjacent pixel circuits coupled to the two OLEDs and the same scan line share one pixel power supply line V_{dd} to receive the pixel power.

[0069] In the pixel circuits of **FIGS. 3 and 4**, the first to eighth transistors **M11a**, **M11b** to **M81a**, **M81b** are formed of the PMOS transistors. However, when the first to eighth transistors **M11a**, **M11b** to **M81a**, **M81b** are formed of the

NMOS transistors, the pixel circuit operates using the waveforms illustrated in **FIG. 6**. Note that PMOS transistors are turned on when the voltage at their gate electrode is lower than the voltage at the source electrode while NMOS transistors are turned on when the voltage at their gate electrode is higher than the voltage at their source electrode. The difference between the gate and source voltages in both cases must be above a threshold voltage of the transistor.

[0070] **FIG. 7** is a circuit diagram illustrating a third embodiment of the pixel circuit used for the light emitting display of the present invention. The third pixel circuit includes two adjacent pixel circuits **110c**, **120c** coupled to one scan line. The left pixel is referred to as the first pixel **110c** and the right pixel is referred to as the second pixel **120c**.

[0071] Each of the first and second pixels **110c**, **120c** include a driving circuit and a switching circuit. The driving circuit **111c**, **121c** includes elements that are coupled to the scan lines s_n , s_{n-1} and are driven by the scan signals s_n , s_{n-1} . The switching circuit **112c**, **122c** includes switching elements that are coupled to the emission control lines E_{1n} , E_{2n} and are driven by the emission control signals e_{1n} , e_{2n} . The switching circuit **112c**, **122c** couples the driving circuit **111c**, **121c** to the OLEDs and controls the flow of current to these OLEDs.

[0072] The first and second pixels **110c**, **120c** share the fourth transistor **M41c** that transmits the initializing signal. Using one initializing transistor decreases the circuit area and increases the aperture ratios of the first and second pixels **110c**, **120c**.

[0073] The source of the fourth transistor **M41c** is coupled to the second OLEDs **OLED21c**, **OLED22c** in the first and second pixels **110c**, **120c**, the drain of the fourth transistor **M41c** is commonly coupled to the capacitor **Cst1c** of the first pixel **110c** and the capacitor **Cst2c** of the second pixel **120c**, and the gate of the fourth transistor **M41c** is coupled to the second scan line s_{n-1} so that the fourth transistor **M41c** transmits the initializing signal in response to the second scan signal s_{n-1} . Therefore, the first and second pixels **110c**, **120c** are simultaneously initialized.

[0074] In the exemplary depiction of the third embodiment shown in **FIG. 7**, the driving circuits **111c**, **121c** of the first and second pixel circuits **110c**, **120c** are similar to the driving circuits **111a**, **121a** of the first and second pixel circuits **110a**, **120a** of the first embodiment. However, the driving circuits of the second embodiment **111b**, **121b** could be used in another example of the third embodiment. As **FIGS. 3 and 4** indicate, one of the differences between the first and second embodiments **110a**, **110b** lies in the location of their respective third transistors **M31a**, **M31b**. Either circuit may be used in the third embodiment, as long as a common fourth transistor **M41c** is also used.

[0075] Further, in the exemplary embodiments of the first, second, and third pixel circuit shown in **FIGS. 3, 4, and 7**, only two emission control lines and two OLEDs are shown per pixel circuit. A plurality of OLEDs may be driven by the driving circuit of each pixel circuit, if an appropriate switching circuit is included and appropriate emission signals are provided.

[0076] As described above, according to the pixel circuit and the light emitting display of the present invention, the

two adjacent pixel circuits coupled to one scan line share one pixel power supply line V_{dd} and a number of OLEDs are coupled to every one pixel circuit. Therefore, it is possible to reduce the number of pixel circuits. It is also possible to reduce the number of wiring lines of the light emitting display. Reducing the number of the pixel circuits and the number of wiring lines both allow an increase in the aperture ratio.

[0077] Although exemplary embodiments of the present invention have been shown and described, it would be appreciated by those skilled in the art that changes might be made in this embodiment without departing from the principles and spirit of the invention, the scope of which is defined in the claims and their equivalents.

What is claimed is:

1. A light emitting display comprising:

an image display unit coupled to a plurality of scan lines, a plurality of data lines, a plurality of emission control lines, and a plurality of first power supply lines, the image display unit including a plurality of pixels formed in regions defined by the scan lines and the data lines,

wherein each of first and second adjacent pixels coupled to one scan line and one first power supply line among the plurality of pixels includes:

first and second organic light emitting diodes;

a driving circuit commonly coupled to the first and second organic light emitting diodes to drive the first and second organic light emitting diodes; and

a switching circuit coupled between the first and second organic light emitting diodes and the driving circuit to sequentially control the driving of the first and second organic light emitting diodes,

wherein the driving circuit includes:

a first transistor for receiving a first voltage from the first power supply line at a gate electrode to selectively supply a current to the first and second organic light emitting diodes;

a second transistor for selectively transmitting a data signal to a first electrode of the first transistor in response to a first scan signal;

a third transistor for selectively diode-coupling the first transistor in response to the first scan signal;

a capacitor for storing the first voltage applied to the gate electrode of the first transistor while a data voltage is applied to the first electrode of the first transistor and for maintaining the stored first voltage in the gate electrode of the first transistor during a period when the first and second organic light emitting diodes emit light;

a fourth transistor for selectively transmitting an initializing signal to the capacitor in response to a second scan signal;

a fifth transistor for selectively transmitting power from the first power supply line to the first transistor in response to a first emission control signal; and

a sixth transistor for selectively transmitting power from the first power supply line to the first transistor in response to a second emission control signal.

2. The light emitting display of claim 1, wherein the first and second adjacent pixels are coupled to different data lines.

3. The light emitting display of claim 1, wherein the first and second adjacent pixels share the fourth transistor.

4. The light emitting display of claim 1, wherein the switching circuit comprises:

a seventh transistor for transmitting the current to a first organic light emitting diode of the first and second organic light emitting diodes in response to the first emission control signal; and

an eighth transistor for transmitting the current to the second organic light emitting diode in response to the second emission control signal.

5. The light emitting display of claim 1, wherein the second scan signal is transmitted to a scan line that precedes the scan line to which the first scan signal is transmitted by one row.

6. The light emitting display of claim 1, wherein the initializing signal is the second scan signal.

7. The light emitting display of claim 1, wherein the initializing signal is a voltage applied to the first and second organic light emitting diodes when no current is generated by the first transistor.

8. A light emitting display having first and second adjacent pixels coupled to one scan line, each of the first and second adjacent pixels comprising:

a first organic light emitting diode and a second organic light emitting diode for receiving current to emit light;

a first transistor having a first drain coupled to a first node, a first source coupled to a second node, and a first gate coupled to a third node;

a second transistor having a second source coupled to a data line, a second drain coupled to the second node, and a second gate coupled to a first scan line;

a third transistor having a third source coupled to the first node, a third drain coupled to the third node, and a third gate coupled to the first scan line;

a fourth transistor having a fourth source coupled to an initializing line, a fourth drain coupled to the third node, and a fourth gate coupled to a second scan line;

a capacitor having a first electrode coupled to a first power supply line and a second electrode coupled to the third node;

a fifth transistor having a fifth source coupled to the first power supply line, a fifth drain coupled to the second node, and a fifth gate coupled to a first emission control line;

a sixth transistor having a sixth source coupled to the first power supply line, a sixth drain coupled to the second node, and a sixth gate coupled to a second emission control line;

a seventh transistor having a seventh source coupled to the first node, a seventh drain coupled to the first organic light emitting diode, and a seventh gate coupled to the first emission control line; and

- an eighth transistor having an eighth source coupled to the first node, an eighth drain coupled to an anode of the second organic light emitting diode, and an eighth gate coupled to the second emission control line.
9. The light emitting display of claim 8, wherein the first and second adjacent pixels share the first power supply line.
10. The light emitting display of claim 8, wherein the initializing signal is transmitted through the second scan line.
11. The light emitting display of claim 8, wherein the first and second adjacent pixels share the fourth transistor.
12. A light emitting display having first and second adjacent pixels coupled to one scan line, each of the first and second adjacent pixels comprising:
- a first organic light emitting diode and a second organic light emitting diode for receiving current to emit light;
 - a first transistor having a first drain coupled to a first node, a first source coupled to a second node, and a first gate coupled to a third node;
 - a second transistor having a second source coupled to a data line, a second drain coupled to the second node, and a second gate coupled to a first scan line;
 - a third transistor having a third source coupled to the first node, a third drain coupled to the third node, and a third gate coupled to the first scan line;
 - a fourth transistor having a fourth source coupled to an anode of the first organic light emitting diode, a fourth drain coupled to the third node, and a fourth gate coupled to a second scan line;
 - a capacitor having a first electrode coupled to a first power supply line and a second electrode coupled to the third node;
 - a fifth transistor having a fifth source coupled to the first power supply line, a fifth drain coupled to the second node, and a fifth gate coupled to a first emission control line;
 - a sixth transistor having a sixth source coupled to the first power supply line, a sixth drain coupled to the second node, and a sixth gate coupled to a second emission control line;
 - a seventh transistor having a seventh source coupled to the first node, a seventh drain coupled to the first organic light emitting diode, and a seventh gate coupled to the first emission control line; and
 - an eighth transistor having an eighth source coupled to the first node, an eighth drain coupled to an anode of the second organic light emitting diode, and an eighth gate coupled to the second emission control line.
13. The light emitting display of claim 12, wherein the first and second adjacent pixels share the first power supply line.
14. The light emitting display of claim 12, wherein the first and second adjacent pixels share the fourth transistor.
15. The light emitting display of claim 12, wherein the initializing signal is a voltage applied to the first organic light emitting diode and the second organic light emitting diode when no current is flowing through the first transistor.
16. A method for driving the light emitting display of claim 12, the method comprising:
- sending a second scan signal having second scan on pulses through the second scan line;
 - sending a first scan signal having first scan on pulses through the first scan line after the second scan on pulse;
 - sending a first emission control signal having first emission on pulses through the first emission control line after the first scan on pulse;
 - sending the second scan on pulse after the first emission control signal on pulse;
 - sending the first scan on pulse after the second scan on pulse; and
 - sending a second emission control signal having second emission on pulses through the second emission control line after the first scan pulse;
- wherein the first scan on pulse, the second scan on pulse, the first emission control on pulse, and the second emission control on pulse are adapted to turn on a transistor having a gate receiving the respective on pulses.
17. A light emitting display having first and second adjacent pixels coupled to one scan line, each of the first and second adjacent pixels comprising:
- a first organic light emitting diode and a second organic light emitting diode for receiving current to emit light;
 - a first transistor having a first drain coupled to a first node, a first source coupled to a second node, and a first gate coupled to a third node;
 - a second transistor having a second source coupled to a data line, a second drain coupled to the second node, and a second gate coupled to a first scan line;
 - a third transistor having a third source coupled to the second node, a third drain coupled to the third node, and a third gate coupled to the first scan line;
 - a fourth transistor having a fourth source coupled to an anode of the first organic light emitting diode, a fourth drain coupled to the third node, and a fourth gate coupled to a second scan line;
 - a capacitor having a first electrode coupled to a first power supply line and a second electrode coupled to the third node;
 - a fifth transistor having a fifth source coupled to the first power supply line, a fifth drain coupled to the second node, and a fifth gate coupled to a first emission control line;
 - a sixth transistor having a sixth source coupled to the first power supply line, a sixth drain coupled to the second node, and a sixth gate coupled to a second emission control line;
 - a seventh transistor having a seventh source coupled to the first node, a seventh drain coupled to the first organic light emitting diode, and a seventh gate coupled to the first emission control line; and
 - an eighth transistor having an eighth source coupled to the first node, an eighth drain coupled to an anode of the

second organic light emitting diode, and an eighth gate coupled to the second emission control line.

18. A method for driving a light emitting display, the light emitting display having an image display unit coupled to a plurality of scan lines, a plurality of data lines, a plurality of emission control lines, and a plurality of first power supply lines, the image display unit having a plurality of pixels formed in regions defined by the scan lines and the data lines, each of first and second adjacent pixels being coupled to one scan line and one first power supply line among the plurality of pixels, each pixel having a plurality of organic light emitting diodes, the method comprising:

receiving a first voltage from the first power supply line to turn on a first switch to selectively supply a current to the plurality of organic light emitting diodes;

selectively transmitting a data signal to the first switch in response to a first scan signal turning on a second switch;

storing the first voltage in a capacitor, while a data voltage is being transmitted through the first switch;

maintaining the stored first voltage to keep the first switch on to transmit the data voltage while the plurality of organic light emitting diodes emit light;

selectively initializing the capacitor in response to a second scan signal;

selectively transmitting power from the first power supply line to maintain the first switch on; and

sequentially controlling driving of the plurality of organic light emitting diodes.

19. The method of claim 18, wherein the first and second adjacent pixels receive the first voltage from a same first power supply line.

20. A method for driving a plurality of organic light emitting diodes of a light emitting display, the organic light emitting diodes being driven by pixel circuits, the pixel circuits being responsive to emission control signals and scan signals, the method comprising:

coupling a pair of adjacent pixel circuits sharing a common scan signal line to one power supply line; and

sequentially switching between organic light emitting diodes coupled to one of the pair of adjacent pixel circuits sharing the common scan signal line driving current from the one of the pair of adjacent pixel circuits sharing the common scan signal line in response to the emission control signals.

* * * * *

专利名称(译)	像素电路和发光显示器		
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申请号	US11/274941	申请日	2005-11-14
[标]申请(专利权)人(译)	KWAK WON KYU 朴成喆		
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摘要(译)

用于发光显示器的像素电路。耦合到一条扫描线的发光显示器的相邻像素共享一条第一电源线。每个像素电路中的驱动电路驱动第一和第二有机发光二极管(OLED)。开关电路耦合在第一OLED和第二OLED与驱动电路之间,以顺序地控制第一OLED和第二OLED的驱动。因为两个相邻的像素电路共用一个像素电源线并且多个OLED耦合到一个像素电路,所以可以减少像素电路的数量和发光显示器的布线数量。其他电路元件也可以在相邻的像素电路之间共享。减少像素电路的布线和其他元件使得可以增加发光显示器的孔径比。

